44900

INSTRUCTION DATA

070677

RFL Industries, Inc., Boonton, New Jersey 07005

44900

Model 66 TEST MODULE

6644

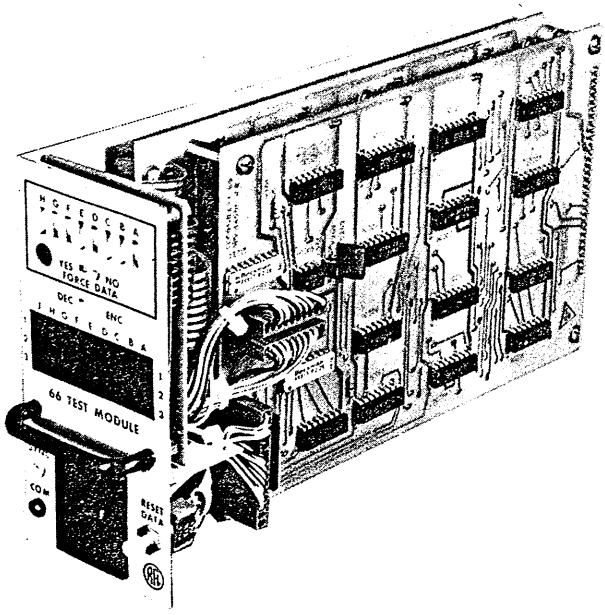


Figure 1. 66 Test Module and Carrying Case.

DESCRIPTION

Model 66 TEST MODULE is one of the RFL 66 TDMS Series of plug-in modules. Its purpose is to provide a visual means to monitor the performance and status of the encoding and decoding process at both ends of a system. It also allows the operator to override the data transmitted in any message word.

The Module may be permanently installed in a Model 68 Chassis, or it can be used as a portable tester and carried to location as needed. The module may be plugged into and removed from operating systems without the need to turn off power or remove them from service. If the module is to be mounted in a Model 68 Chassis, five standard one-half-inch increments in the chassis must be allocated. However, only one increment need be allotted if the 66 TEST MODULE will be used with a 68 EXT Extender Board.

SPECIFICATIONS

Ambient Temperature: −30 to +70°C.

Power: 11 to 13 Vdc @ 220 mA.

Size: Five standard one-half-inch module spaces in an RFL Model 68 Chassis.

OPERATION

General Information

Figure 2 shows the coded message structure used in the 66 TDMS. Each message begins with a header followed by single, double or triple scanned data words. Each data word contains eight information bits and an odd parity bit. The Test Module can be used at the encoding (or sending) end of the system to display the eight data bits and the parity bit for any word in the message, depending upon the setting of the thumbwheel switches. It can also be used to override the normal data bits in the selected word and can force a different pattern by setting the toggle switches at the top of the module. At the decoding (or receiving) end of the system, the eight data bits received and decoded by the decoding controllers can be displayed.

Figure 3 is an interconnect diagram showing how the Test Module is wired into a system. The system will work normally with or without the Test Module plugged in. Whenever the module is used at the encoding end of the system, the light-emitting diode (LED) lamps display the status of the data on the SERIAL DATA OUT line, Terminal 20 of the 66 ENC/L. That is the signal line which actually keys the tone transmitter. However, when the data is forced, the signal going into Terminal 22 of the 66 ENC/L through the 1K resistor is overpowered by the Test Module. That is the data line just prior to the encoding process. At the receiving end of the system, the data to be displayed is picked off the busses which are the outputs of the decoding controllers. These signals have been decoded.

The other signals in Figure 3 are required to make the Test Module work, or they will be described in detail later on. There are two spares. These are wired to other signals in the system at the discretion of the system design engineer. It will be necessary to review the drawings of each individual system to determine where these spares are wired.

Words in the message are selected by the thumbwheel switches. Each switch has 16 positions and so the words are identified by a hexadecimal (base 16) code. In base 10 arithmetic the characters are 0 through 9 but in base 16 or hexadecimal arithmetic, the characters are 0 through 9 and A through F. Thus the sequence is as follows:

0
1
2
3
4
5
6
7
8
9
A
B
C
D
E
F

A message word to be displayed is selected by a "double-digit" hexadecimal code. For example the first word in the message is "00", the fifth word is "04", the fourteenth word is "0D" and the forty-fifth word is "2C".

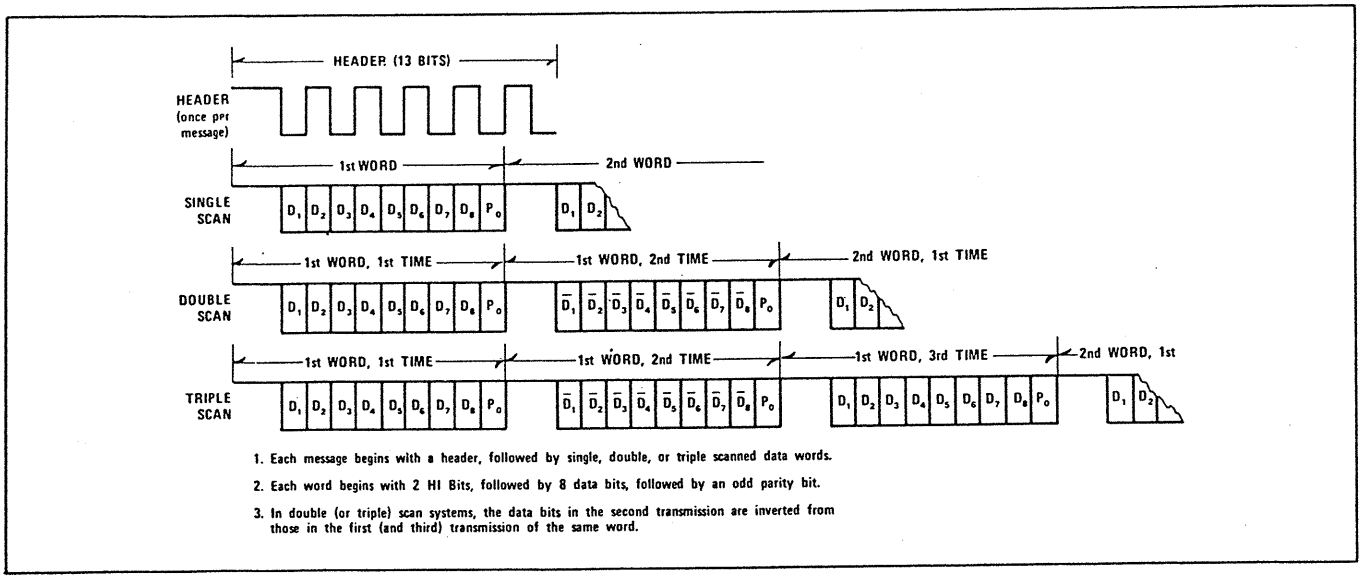


Figure 2. RFL 8-11 Code Format.

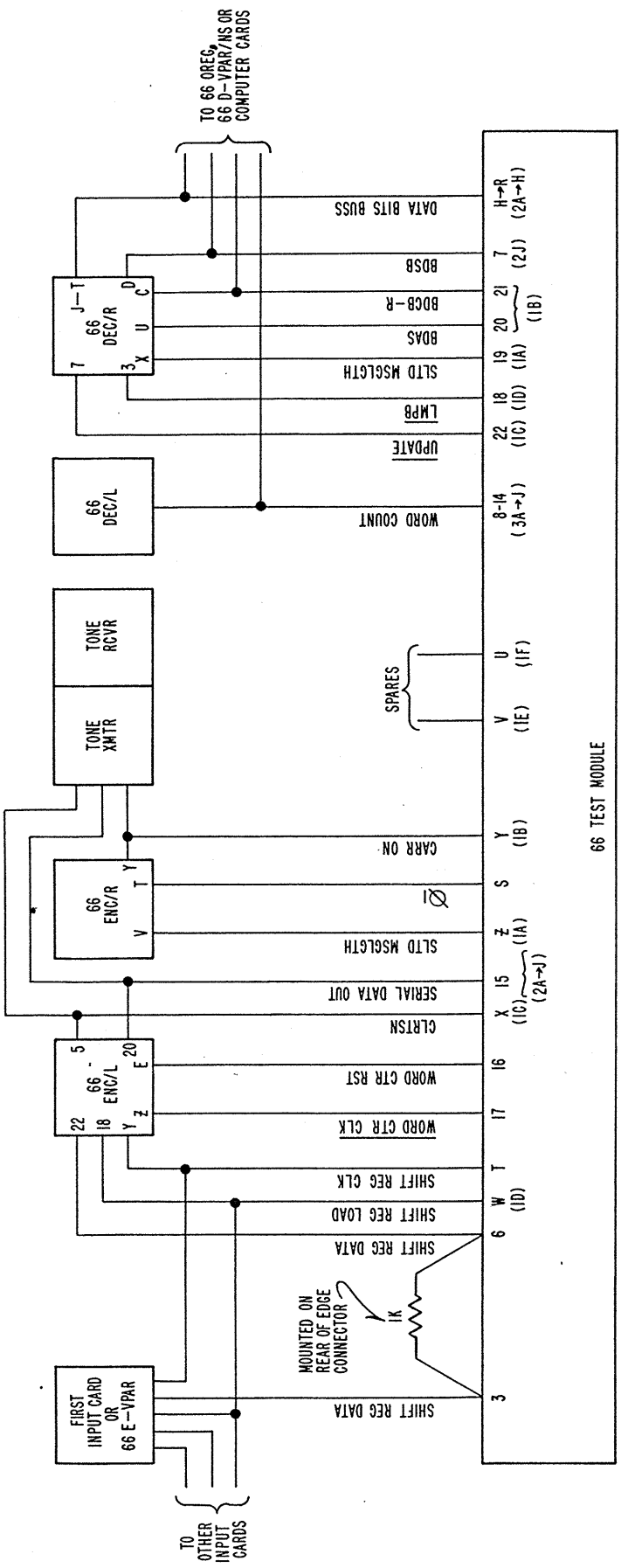


Figure 3. System Interconnect Wiring.

Monitoring the Encoder

Figure 4 shows the front panel set up to monitor the encoding controller output. The DEC-ENC switch is in the ENC position and the FORCE DATA switch is in the NO position. With the FORCE DATA switch in the NO position, the upper row of switches is inactive and the FORCE DATA light will be off.

Row 2 shows the actual status of data bits D1 through D8 and the parity bit in the selected word. These are read in order from right-to-left. The lamps light when bits are logic ones. Each time Row 2 updates, that is, each time the selected word is sampled for display, the 3J lamp will blink. The RESET DATA switch in the lower right-hand corner of the panel causes Row 2 to blank until the next time it is updated.

The RESET DATA switch is most useful in non-scanning type systems. For example, suppose the thumbwheel switch is changed. Since it may be a long time before the next message is transmitted, the RESET DATA switch can be pushed to blank the display. Now it is not necessary to remember the current display status and look for a change. The display will be dark, and the next time any lamp lights, it will be as a result of the next message.

The lamps in Row 3, columns A to G, display the word counter's status. The word counter is used by the encoding controllers to know which word in the message they are encoding. These lamps turn on and off fast in many systems because of the high transmission speed, and they may appear as a blur. However, the fact that they blink at all usually means the counter is counting. The counter counts in binary code (base 2 arithmetic). Lamp 3A displays the least-significant bit, and 3G shows the most-significant bit. The counter counts only as high as the maximum number of words in the message.

Lamps 1F and 1E are used to monitor the status of the spare inputs at Terminals U and V respectively. It will be necessary to review the drawings for each individual system to determine where these spares may be wired and what signals they are monitoring.

Lamp 1D will change states and alternately turn on and off each time a shift register load pulse is developed by the encoding controllers. This pulse is developed just prior to the sending of each message. It is used to tell the input cards in the system to accept new information. If this lamp does not flash in scanner systems or, in non-scanning systems, if this lamp does not change state each time the encoding controllers are instructed to send a message, then either the encoding controllers are defective or they are not receiving the proper input to send a message. If the encoders are working at all, and are able to send a message, but the 1D lamp is not responding, it is likely that the message being sent contains all logic ones or zeros.

Lamp 1B displays the status of the CARR ON signal out of the encoding controller. This is the command which, if so connected, tells the tone transmitter to turn on. Lamp 1C monitors the CLEAR-TO-SEND response from the tone transmitter.

The CLEAR-TO-SEND signal will become true a short time after the tone transmitter is told to come on. This delay allows time for the transmission medium to stabilize before a message is sent. These lamps are most useful in systems where the tone transmitter is keyed on and off, such as polled systems. For systems where the tone is on continuously, the system engineer may use these two lamps as spares to monitor other signals.

Finally lamp 1A shows the status of the SELECTED MESSAGE LENGTH. This light shows whether the encoding controllers are sending a short or a long message. Many systems, however, use only single-length messages so that all messages have the same number of words and bits. For such cases, this lamp can also become a spare.

Forcing Encoder Data

The Test Module can be used to override the normal data transmitted for any word in a message. *This can be a hazardous feature if a false or undesirable control action can result at the receiving end.* The FORCE DATA switch should be in the NO position whenever the Test Module is inserted into or removed from a chassis, whenever the encoder is not to be forced, or whenever the decoding end of the system is to be monitored. Extreme care should be exercised by the operator when forcing data in a system where the receiving end of the system controls machinery. If possible those end devices should be disabled before attempting to force data.

To force the data, select the word in the message to be forced (and simultaneously displayed) with the thumbwheel switch, set the eight switches across the top of the module to the desired pattern (up = logic 1) and throw the FORCE DATA switch to the YES position. Row 2 of the lamps will then display the actual data bits being sent as usual. See Figure 4. To discontinue forcing the data, return the FORCE DATA switch to the NO position.

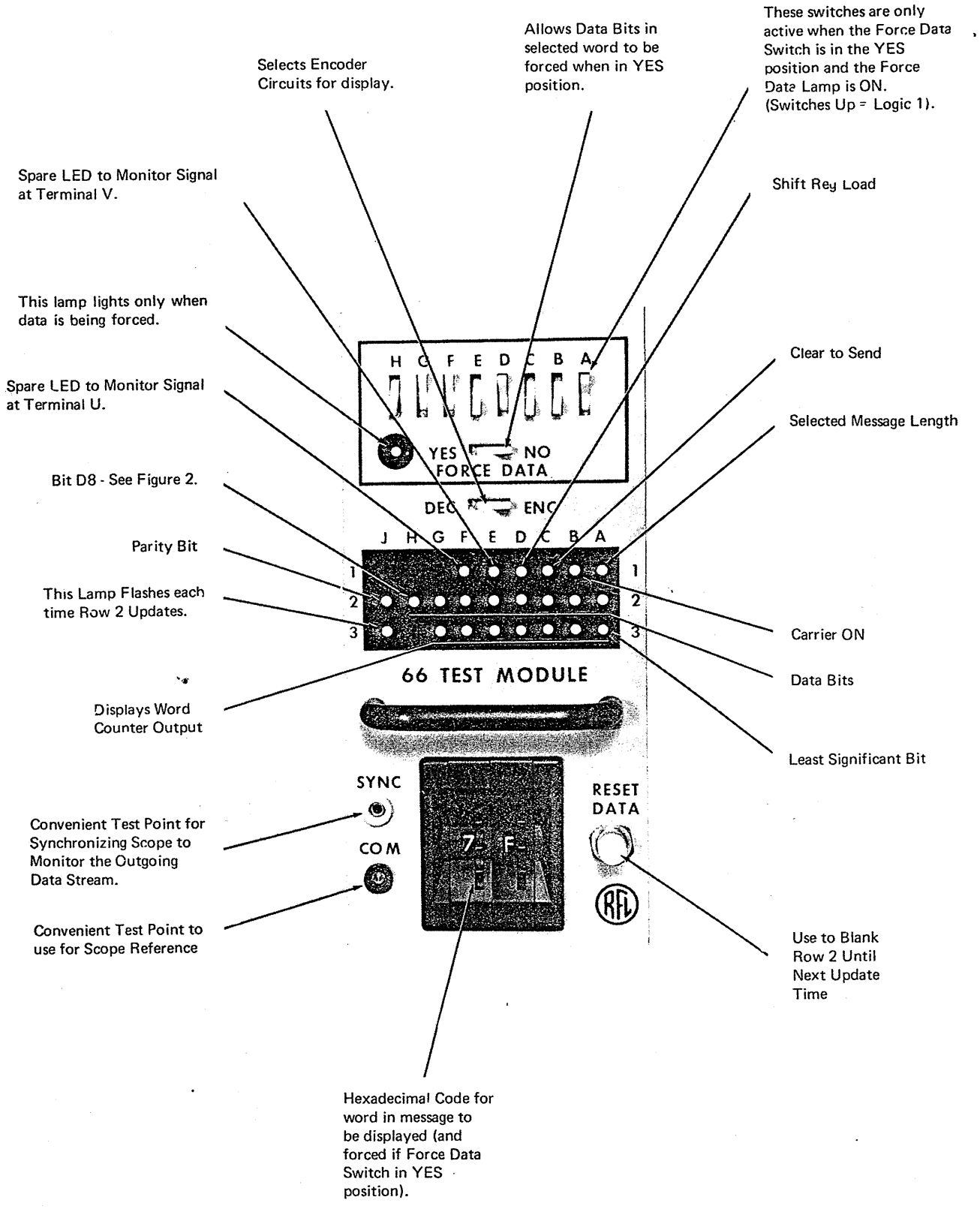


Figure 4. Monitoring or Forcing Encoder Data.

Monitoring the Decoder

Figure 5 shows the front panel set up to monitor the decoding controller output. The DEC-ENC switch is in the DEC position and the FORCE DATA switch is in the NO position. The upper row of switches is inactive and the FORCE DATA light will be off.

Row 2 displays the actual status of data bits D1 through D8 and an error-detection bit which will light when the decoding controllers detect an error in the selected word. These are read in order from right-to-left. The lamps light when the bits are logic ones. Each time Row 2 updates, that is, each time the selected word is sampled for display, the 3J lamp will blink. The RESET DATA switch in the lower right hand corner of the panel causes Row 2 to blank until the next time it is updated.

The lamps in Row 3, columns A to G, display the word counter's status. The word counter is used by the decoding controllers in a manner similar to that described for the encoder.

Lamps 1F and 1E are used to monitor the status of the spare inputs at Terminals U and V respectively. It will be necessary to review the drawings for each individual system to determine where the spares are wired and what signals they are monitoring. The status displayed on these lamps does not depend upon the position of the DEC-ENC switch.

Lamp 1D will change states and alternately turn on and off each time a $\overline{\text{LMPB}}$ pulse occurs. The decoder puts out this pulse after each word in the message has been received. If this pulse is not being outputted, then the 66 OREG cards cannot be loaded with new information. These pulses are generated only after a message header has been detected, and they stop after the proper number of words has been received. Thus, in non-scanning systems where messages come only once in a while, Lamp 1D will flash only when a header has been detected and a message is being received.

Lamp 1C will change state and alternately turn on and off each time the decoding controllers detect the end of a message. The lamp is triggered by the $\overline{\text{UPDATE}}$ pulse.

Lamp 1B shows BDAS status. This lamp will light as soon as an error in any word is detected by the decoding controllers or by other error detection circuits, such as a vertical parity detector, if used. Once this lamp is lit, it will remain so until the next time a message header is detected.

Lamp 1A shows the status of the SELECTED MESSAGE LENGTH. This lamp shows whether the decoding controllers have received a short or a long message. But, as was described for the decoders, many systems use only single-length messages so that all messages have the same number of words and bits. For such cases, Lamp 1A can also be used as a spare.

Troubleshooting Tips

The following troubleshooting suggestions are offered as ideas to get started.

If possible, end devices should be disabled to prevent accidental actuation of control circuits.

Monitor each word coming out of the encoding end of the system. If it is possible to actuate the inputs to the input cards associated with the encoder, this should be done. If it is not possible to actuate the inputs, then the inputs should be measured with a scope or voltmeter. If the encoding end of the system is working, the lamps in Row 2 will follow the inputs.

If the lamps do not dollow the inputs, then force data. The lamps in Row 2 should follow the toggle switches at the top of the front panel on the Test Module. If the, lamps do track the force-data-switch status, then the encoding controllers are probably working. The trouble is most likely to be with the input cards, the input wiring, or the actual input devices (switches, relays, a/d converters, etc.).

If the logic at the encoding end of the system appears to operate satisfactorily, the output of the tone transmitter can be monitored with a scope or a suitable set of earphones to verify that the tone is changing frequency. Likewise the tone at the decoding end should be monitored to verify that a changing tone is being received.

At the decoding end, the Test Module can be used to monitor the received message words. If the Test Module does not show flashing lamps at 1D and 1C then the decoder has not detected a message coming in. If Lamp 1B or 2J is blinking or on steady, then errors are being detected in the incoming messages. In either case, it may be worthwhile to look at the data output from the tone receiver to ascertain that data is coming out, that the bias has been adequately adjusted, that the data stream does not have excessive jitter and that the carrier-fail signal indicates the carrier is present. If the tone seems OK, then it is possible the decoding controllers are defective.

If the incoming data is known, then each of the incoming data words as displayed on Row 2 should be checked for a match. If a match is obtained, then there may be problems in the OREG cards or with the cards following the OREG cards in the system (such as DE16 cards, CMDEC cards, or relay cards) or in the end device being controlled. If data does not match, the decoding controllers may be at fault.

THEORY OF OPERATION

The schematic diagram of the test module is shown in Figures 6, 7, 8, and 9. Figure 8 shows the electronics on the main or lower PC board. Figure 9 shows the electronics on the secondary or upper level PC board. Figure 6 is the schematic which shows the light-emitting diodes and switches on the PC board mounted behind the front panel of the

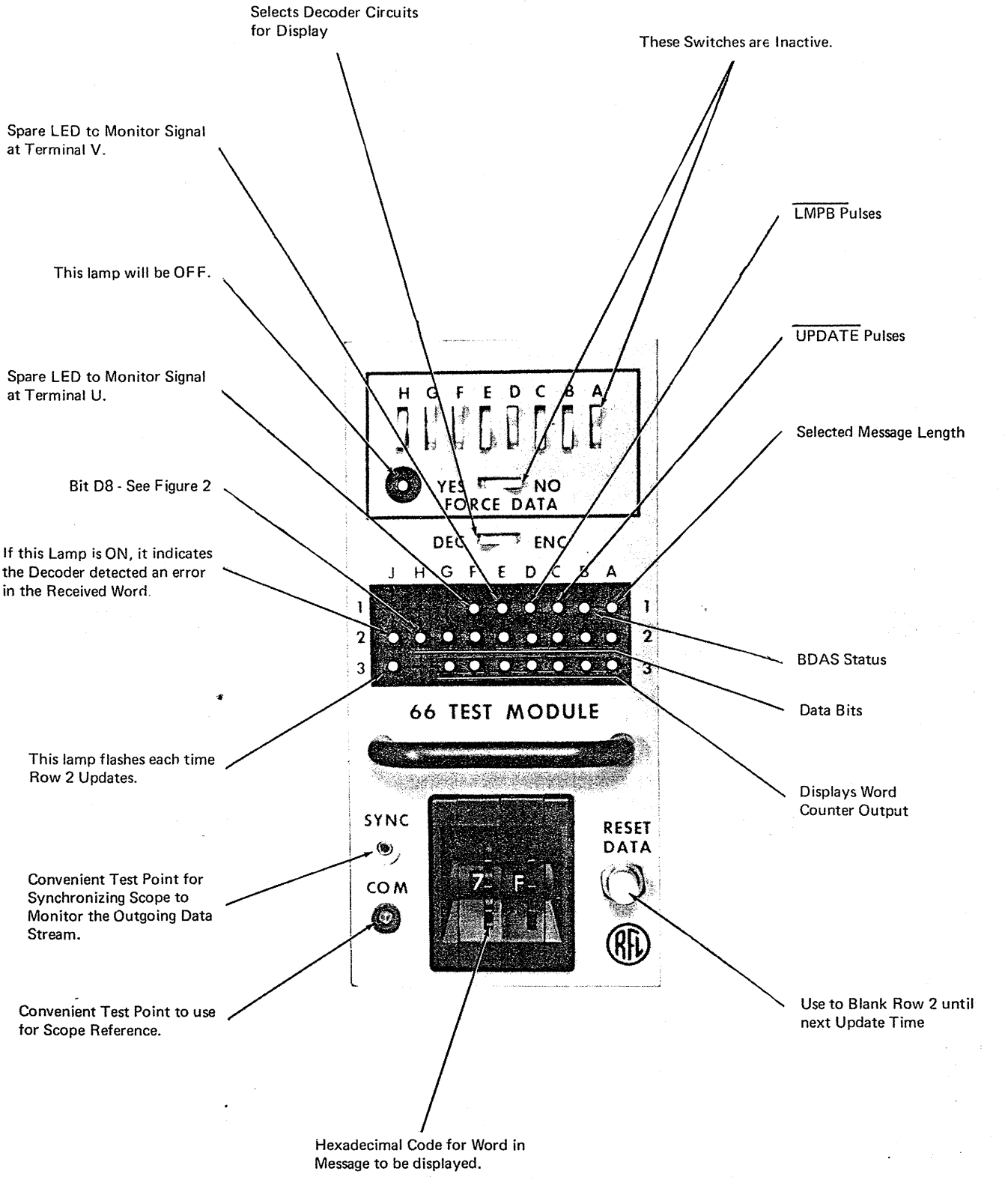


Figure 5. Monitoring Decoding Data.

test module, and Figure 7 shows the wiring for the switches and test jacks which are mounted on the front panel.

The lower circuit board, which is called the main board, contains the input protection diode networks CRZ101 thru CRZ104. Each of the hexagons in Figure 8 represents a pin connection to one of the diode networks. Each pin has two diodes associated with it. These diodes are normally reversed biased except when they are connected to a voltage source which is less than the Common potential or greater than the positive supply voltage. The purpose of these networks is to prevent excessive input voltage to the integrated circuits on the main and secondary boards.

In the upper left-hand-corner of Figure 8 where Wires 2 and 3 of Ribbon Cable C are connected, are shown the connections to the DEC-ENC switch. When this switch is in the ENC position, the voltage on Wire 3 will be +12 volts and all connections labeled K_b will be at a logic 1. All connections to points identified as K_a will be at a logic 0.

When K_b is high, the B inputs to IC109 will be gated through to the D outputs. Thus the status of the SHIFT REG LOAD, CLTSN, CARR ON, and SLTD MSGLGTH KB signals are connected through IC109 to the lamp driver, IC108. Notice that IC110B is connected in a divide-by-two configuration which would cause Lamp 1D to alternate states each time the SHIFT REG LOAD pulse occurs.

When the K_a line is high, to monitor the decoder, the signals at Terminals 18 through 22 will be gated through the A inputs of IC109. The $\overline{\text{LMPB}}$ signal is divided by two in IC110B just as the $\overline{\text{SHIFT REG LOAD}}$ pulse was for the encoder. Also, the $\overline{\text{UPDATE}}$ signal is likewise divided by two in IC110A. IC111A and IC111B are interwired to form a set-reset flip-flop. They are used to capture a short BDAS pulse at Terminal 20 which might otherwise be of too short a time duration for the human eye to respond. That flip-flop is reset by the BDCB-R pulse which is generated by the decoder when it detects the receipt of a message header.

Most of the remaining logic on Figure 8 is used to force encoder data. At the bottom of the schematic is indicated how a 1K resistor is to be wired externally on the edge connector and in series with the data-output signal from the first input card. The function of the 1K resistor is to limit the current out of the input card to no more than 12 mA when data is being forced. The actual data signal is overpowered by turning on either Q101 or Q102. Q101 is used to generate logic ones and Q102 is used to generate logic zeros. If the output of IC102B is high, it will be permissible for the Test Module to force data, and logic gates IC102D and IC104C will be enabled. The output of IC102D will be high when it is desired to force a logic zero and the output of IC104C will be low when it is desired to force a logic one. IC104C and IC102D cannot both be on at the same time. Which is active is controlled by the output from IC101 at Pin 3. IC101 is a parallel-in, serial-out, 8-bit shift-register. It is loaded from the data switches on the front panel at the same instant in time as the normal system input cards are loaded.

The activation of IC102D and IC104C as well as the clocking for shifting of IC101 is inhibited until the voltage at IC102B-6 becomes a logic one as a result of the word counter's output coinciding with the setting of the thumbwheel select switch. If the DEC-ENC switch is in the ENC position and if the FORCE DATA switch is ON, then the output of IC102A will be high. This signal says that the encoder can be forced when the proper word is selected, and it is the other input to IC102B at Pin 5.

The SHIFT REG CLOCK signal from the encoding controller enters the Test Module at Terminal T and is buffered by IC103C and IC103B. This signal then goes to three places. It goes upstairs through Wire 24 of Ribbon Cable A, it goes to IC102C-8 to clock the IC101 shift-register and it goes to the clock input of IC105.

The output of IC107A at Pin 3 will be a pulse which is gated through IC104A when the DEC-ENC switch is in the ENC position. From there it goes through IC104B and is gated at IC107C with the signal that means the word counter's output and the setting of the thumbwheel switch agree. The output of IC107C is used to load the memory registers on the secondary board. IC107A-3 will pulse once for each unique word in the message. IC105 is a binary counter which is reset either by a SHIFT REG LOAD signal or by the signal from the encoding controller which causes the word counter to be incremented. IC105 is then able to count SHIFT REG CLOCK pulses. After 8 pulses have been counted, IC105-6 goes high. At the next phase-1 pulse from the encoder (which will have occurred after the eighth data bit in the message word is available at the output of the encoding controller to key a tone transmitter) IC107B-4 will go high and IC111C-10 will go low. Since the output of 106A-1 is also high, a pulse will appear at IC107A-3. When the phase-1 pulse returns to 0, IC107B will go low, and IC111C-10 will go high clocking the 0 at IC106A-5 to the Q output at Pin 1 and causing IC107A to be disabled until the next pulse from IC111D-11. Thus the memory registers on the secondary board are loaded only at the correct instant in time and only during the first scan in a single or multiply scanned message.

When K_a is high, representing that the decoder is being monitored, $\overline{\text{LMPB}}$ pulses which are inverted by IC103E are gated through IC104D, IC104B and IC107C to load the memory registers on the secondary board when the correct word, as selected by the thumbwheel switch, is available to the Test Module.

Referring now to Figure 9, the schematic of the secondary board, IC202, IC203 and IC209B are used as a 9-bit memory register to store the status to be displayed between update times. IC208, IC204 and one fourth of IC210 are used as a 9-pole, 2 position, electronic switch to gate either encoder or decoder information into the 9-bit memory register. When monitoring the decoder output, data is taken directly from the data-bit busses at the output of the decoding controller. However, when monitoring the encoder, the serial data stream at its output must be captured and converted to parallel information. That is the function of IC207A and IC207B which is a serial-in,

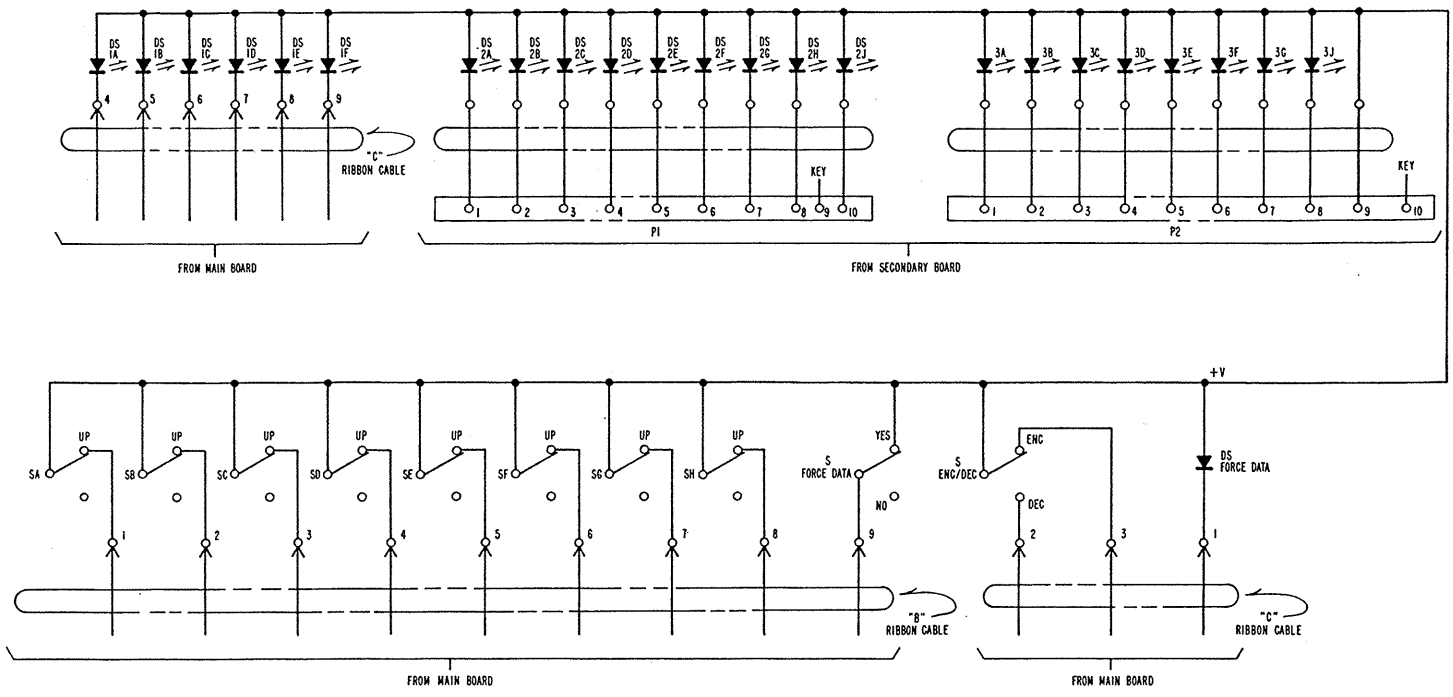


Figure 6. Display Board Schematic.

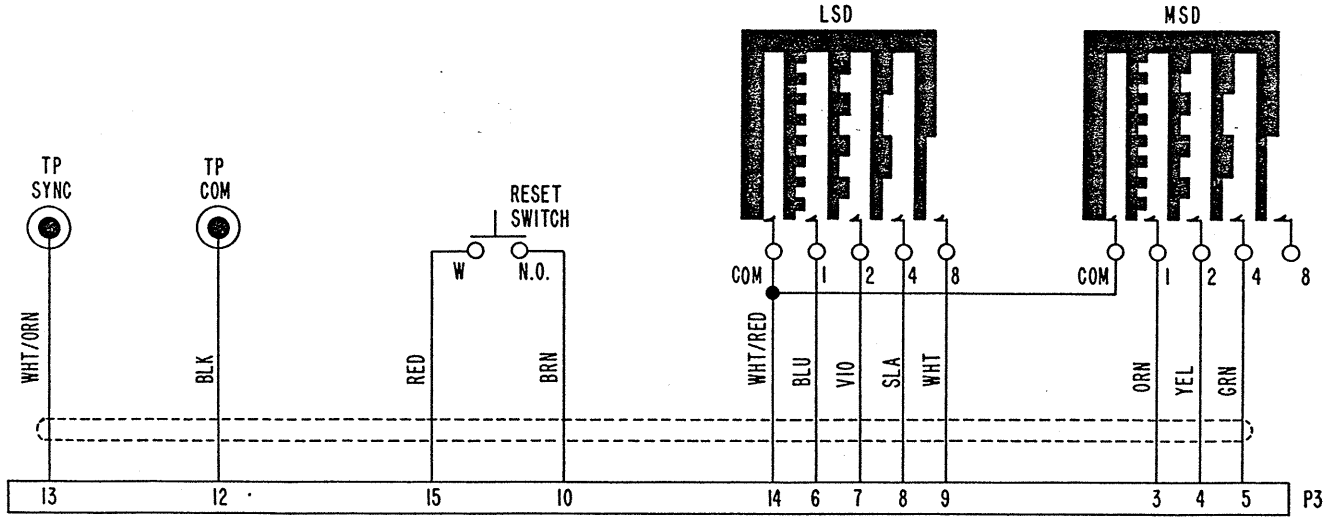
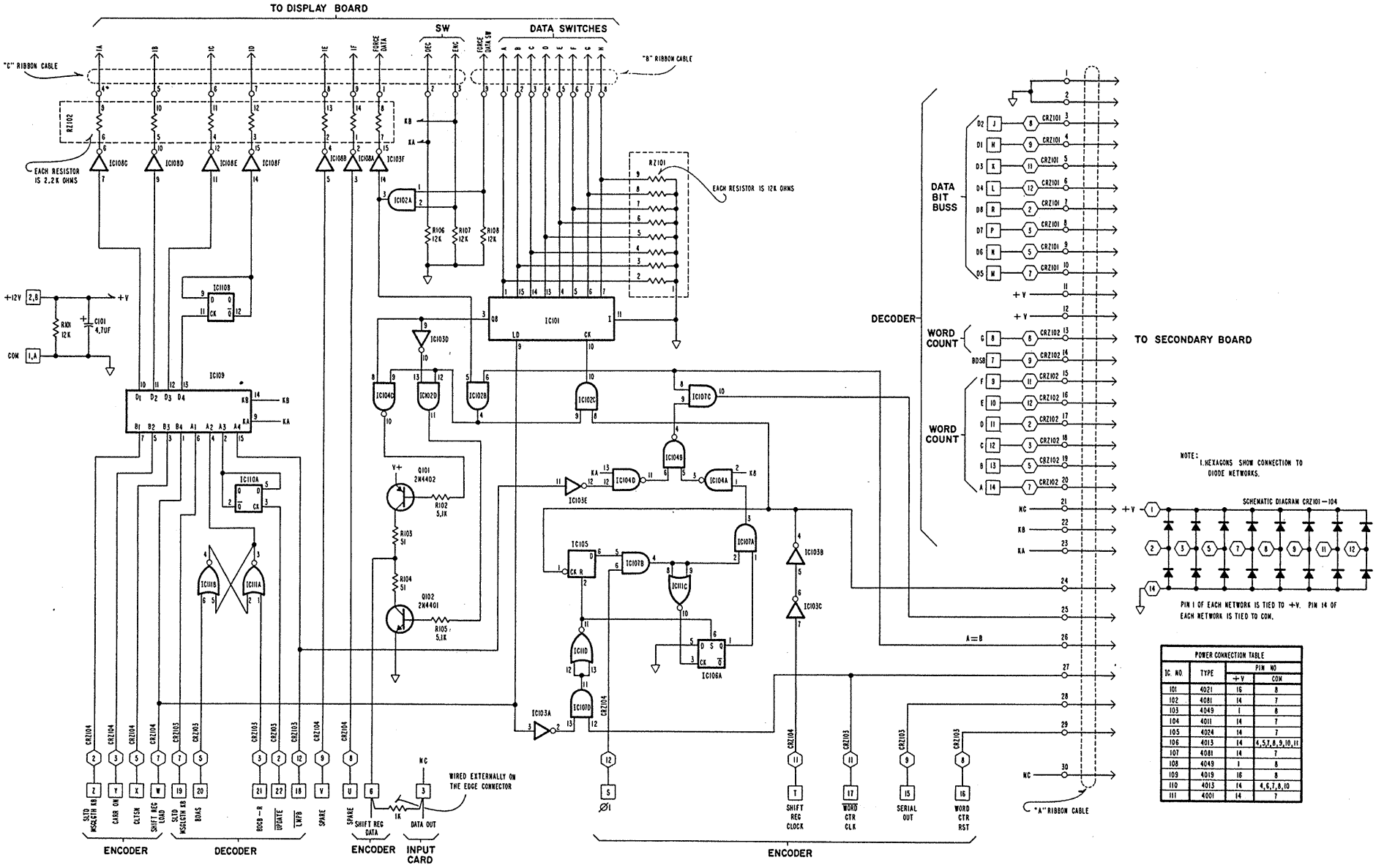


Figure 7. Panel and Switch Assembly Schematic.



POWER CONNECTION TABLE			
IC NO	TYPE	PIN NO +V	PIN NO COM
101	4021	16	8
102	4081	14	7
103	4049	1	8
104	4011	14	7
105	4024	14	7
106	4013	14	4,5,7,8,9,10,11
107	4081	14	7
108	4049	1	8
109	4019	16	8
110	4013	14	4,6,7,8,10
111	4001	14	7

Figure 8. Main Board Schematic.

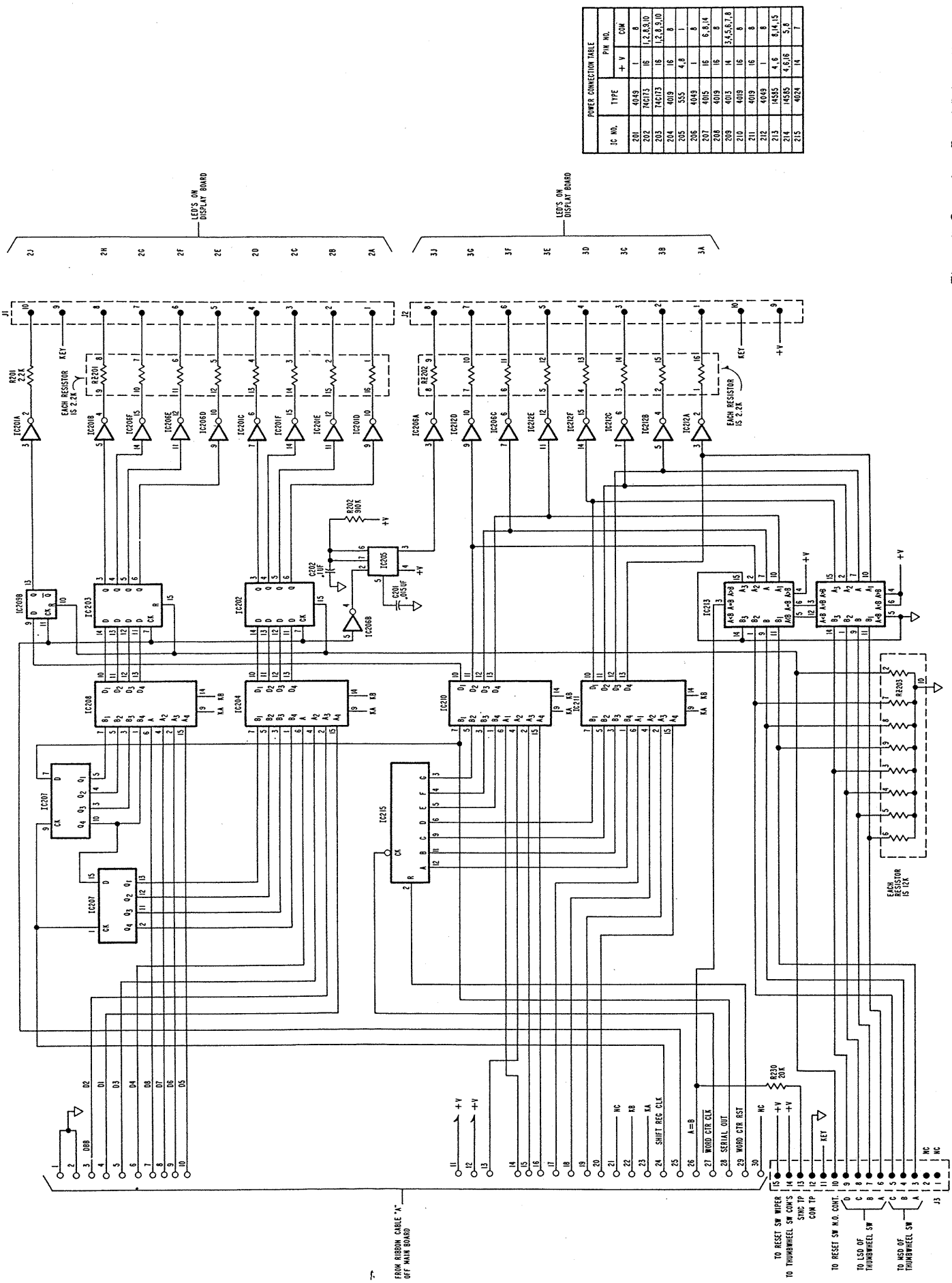


Figure 9. Secondary Board Schematic.

parallel-out 8-bit shift-register. Its input is the serial data stream at the output of the encoding controller. It is clocked by the SHIFT REG CLK signal out of the encoder.

Three fourths of IC210 and all of IC211 are used as a 7-pole, 2-position electronic switch to gate either encoder or decoder word-count information to the lamps on the front panel for display. When the K_a signal is high, the parallel outputs from the decoding controller's word counter will be gated through to the display lamps in Row 3 and to the digital comparators IC213 and IC214. When K_b is high, the output of IC215 is displayed and made available to the comparators. Since the word-counter outputs in the encoding controller are not all available as parallel information, the counter IC215 is used to generate the proper binary code.

The comparators IC213 and IC214 compare the respective word-counter output with the thumbwheel-switch setting. When these two agree, Pin 3 of IC213 will be at a logic 1. This signal is available to the SYNC test jack on the front panel. It is protected, however, by the 20K resistor R203.

IC205 is a monostable pulse generator which generates tenth-second pulses to cause Lamp 3J to blink each time the 9-bit memory register is updated.

PARTS LIST

CIRCUIT SYMBOL	DESCRIPTION	PART NUMBER
	Model 66 TEST Module, Assembly HB-44900	
C101	Capacitor, tantalum, 4.7 μF, 20%, 20V, Kemet T324B475M020AS, or eq.	H-1007-711
C201	Capacitor, ceramic, 0.015 μF, 10%, 50V, Type CK05, Spec HA-38309	H-0100-16
C202	Capacitor, metallized polyester, 0.1 μF, 10%, 250V, Seacor 106-0.1, or eq.	H-1007-1255
CRZ 101 thru 104	Silicon 16-diode array, Texas Inst. T1D125, or eq.	HA-45484
IC101	8-Stage static shift register, RCA CD4021AE, or eq.	H-0615-36
IC102, 107	Quad, 2-input AND gate, RCA CD4081BE, or eq.	H-0615-31
IC103, 108, 201, 206, 212	Hex Inverter - buffer, RCA CD4049AE, or eq.	H-0615-7
IC104	Quad, 2-input NAND gate, RCA CD4011AE, or eq.	H-0615-5
IC105, 215	7-Stage binary counter, RCA CD4024AE, or eq.	H-0615-14
IC106, 110, 209	Dual, D-type flip-flop, RCA CD4013AE, or eq.	H-0615-1
IC109, 204, 208, 210, 211	Quad, AND-OR select gate, RCA CD4019AE, or eq.	H-0615-37
IC111	Quad, two-input NOR gate, RCA CD4001AE, or eq.	H-0615-3
IC202, 203	TRI-STATE, quad, D-type flip-flop, National MM74C173N, or eq.	H-0615-43
IC205	Linear functional block, National LM555CN, or eq.	H-0620-108
IC207	Dual, 4-stage shift register, RCA CD4015AE, or eq.	H-0615-25
IC213, 214	4-Bit magnitude comparator, Motorola MC14585CP, or eq.	H-0615-39
Q101	Transistor, silicon, PNP, Type 2N4402	HA-29099
Q102	Transistor, NPN, Type 2N4401	HA-42574
R101-108, 201-203	Resistor, fixed, composition, 5%, ¼W, value on schematic, Allen Bradley CB, or eq.	H-1009-(xxx)
RZ101, 201, 202	Resistor network 12K, 2%, 9 resistor, 2.7 w/pkg., Beckman Resnet 785-1-R12K, or eq.	HA-45440
RZ102, 203	Resistor network 2.2K, 2%, 8 resistors, 1.5 w/pkg., Beckman 898-3-R2.2K, or eq.	HA-45441
----	Schematic, main board (Figure 8)	HE-44904
----	Schematic, secondary board (Figure 9)	HE-44907
----	Schematic, display board (Figure 6)	HD-44917
----	Schematic, panel and switch assy. (Figure 7)	HD-44914